Editorial

Asynchronous architecture

Asynchronous design is enjoying a worldwide resurgence of interest following several decades in obscurity. Many of the early computers employed asynchronous design techniques, but since the mid 1970s almost all digital design has been based around the use of a central clock. The clock simplifies most aspects of design and offers methodologies which are straightforward and easy to automate. These benefits have helped digital engineers to take advantage of the ever-expanding resource at their disposal, while keeping design costs under control. Comprehensive CAD systems used pervasively in industry, and targeted specifically at synchronous design styles, are one way of achieving this.

If the clock has brought these advantages, and the CAD systems available commercially are targeted at clocked circuits, why are we considering abandoning the clock? The answer to this question is based upon a number of observations relating to developments in the base technologies, the markets the products are sold into, advances in the alternatives to clocked design and the CAD support for those alternatives.

First, the technology used to build digital systems continues to advance, with ever more transistors on a chip. As process technology continues to shrink individual transistors, the ratio between wiring and logic delays changes, with wiring moving into dominance. Clocked design requires a single signal, the clock, to be detected at the same time everywhere on the chip, and any deviation from perfect synchronicity (clock 'skew') adds overhead to the logic delays. Asynchronous design is based on local control, so, as the wiring delays increase in proportion to the gate delays, the performance balance swings away from the clock towards asynchronous control.

Secondly, computing is becoming increasingly portable. Laptop computers are visible evidence of this, but other products such as digital mobile telephones, pagers, electronic diaries and personal digital assistants also conceal considerable computing power. Battery life is an important specification point for all of these products, and the relentless beat of a clock causes the electronics to consume more power than is strictly required to fulfill its function. These products also tend to rely on radio communications, and the clock maximises the interference potential of the digitial circuits which are contained within the same small package as the sensitive analogue radio circuits. Asynchronous design offers the potential of reduced power consumption and better electromagnetic compatibility.

Thirdly, although there has been little commercial use of asynchronous techniques during the last few decades, academic research has continued at a low level and has delivered advances in techniques and tools which promise to remove many of the historic difficulties of the approach.

Although asynchronous techniques are applicable across a wide range of circuits, this Special Section is dedicated to the design of asynchronous processors. Microprocessors are, perhaps, the most highly developed digital circuits, and therefore the most demanding application for asynchronous techniques. Furthermore, the organisations used in modern microprocessors to achieve very high performance are firmly rooted around synchronous pipelines, and many techniques do not transfer readily to the asynchronous domain. Therefore, designers of asynchronous processors have to take a step back and view the problem from a different perspective, often developing new techniques and sometimes finding approaches which benefit from the more flexible design environment offered by asynchronous control. The general purpose processor papers presented here explore decoupled execution (University of Utah), a novel 'rotary' pipeline organisation (University of Cambridge) and superscalar instruction issue (University of Manchester). All these designs have a strongly asynchronous flavour to their architectural approach. Asynchronous techniques can also be exploited in the special-purpose processor area, as in the paper on image filtering (France Telecom), and are applicable to programmable logic (University of Edinburgh).

The remaining papers in the Section describe aspects of asynchronous processor design, such as design methodologies (University of Surrey), verification of datapath circuits (University of British Columbia), and a novel binary addition circuit (University of Columbia).

We believe that the papers in this Special Section represent an interesting snapshot of current research into applications of asynchronous design styles in demanding domains. We hope that you will also find them interesting, and that they might both offer insight into current asynchronous ideas, and inspire additional research in the area. There are certainly many challenging problems still to be solved!

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IEE Proceedings online no. 19960812

Erik Brunvand received his PhD in computer science from Carnegie Mellon University, Pittsburgh, PA, in 1991. He is currently an Associate Professor in the Department of Computer Science at the University of Utah, Salt Lake City. His research interests include asynchronous and self-timed circuit and system design, and automatic compilation of asynchronous systems from program descriptions. He is also interested in computer architecture, VLSI, and in how asynchronous systems can find a niche in these areas. He has recently been involved in the organisation of a series of conferences related specifically to asynchronous and self-timed design. The Async94 conference, held in Salt Lake City, has been followed by Async96 in Japan, and Async97 in The Netherlands.

Steve Furber is the ICL Professor of Computer Engineering in the Department of Computer Science at Manchester University. Prior to this appointment he was in charge of the hardware development group within the R&D department at Acorn Computers Ltd, and was a principal designer of the BBC Microcomputer and the Acorn RISC Machine (a 32-bit RISC microprocessor for low-cost applications), both of which earned Acorn Computers a Queen's Award for Technology. He also led the team which developed the hardware architecture and VLSI components for the Acorn Archimedes. Since moving to the University of Manchester in 1990 he has established a research group with interests in asynchronous logic design, and has secured European and UK government funding to develop asynchronous design methodologies within a range of industrial collaborative projects. One result of this work has been the AMULET1 processor, designed within the ESPRIT Open Microprocessor systems Initiative OMI-MAP project, which was recognised with a 1995 British Computer Society Award and the 1995 'Computing' IT Gold Award for Technology Transfer.

Takashi Nanya received BE and ME degrees in mathematical engineering and information physics from the University of Tokyo, Tokyo, Japan, in 1969 and 1971, respectively, and his DrEng degree in electrical engineering from Tokyo Institute of Technology, Tokyo, Japan in 1978. From 1971 to 1981, He was a research staff member of NEC Central Research Laboratories where he worked on asynchronous logic synthesis. Since 1981, he has been a faculty member of Tokyo Institute of Technology and is now a professor in the Department of Electrical Engineering. Since 1995, he also has been a professor in the Department of Mathematical Engineering and Information Physics at the University of Tokyo. He was a visiting research fellow at Oakland University, Michigan in the fall quarter of 1982, and at Stanford University, California in the 1986-87 academic year. His research interests include fault-tolerant computing, computer architecture, design automation and asynchronous computing. He received the Best Paper Award from IEICE in 1987. He served as program co-chair of the 1994 IEEE International Symposium on Fault-Tolerant Computing and as conference co-chair of the 1996 IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems.